PC03XT
Time Code Reader

User's Guide
April 1997

CHAPTER ONE
INTRODUCTION

1.0 GENERAL

The PC03XT Time Code Reader Module is a full length XT module designed to decode time code signals in either an IBM PC XT/AT Computer environment or in Datum's M80XT Controller Chassis.

The software interface (described in Section Two) consists of setup parameters, time requests, time code data transfers, and interrupts.

The hardware interface (described in Section Three) consists of a I/O connectors (four BNC connectors or 15 Pin "D" connector) located on the rear panel support bracket, a Peripheral Data Connector used for interfacing the module to other Datum products, and the PC bus interface used to interface the module to a IBM PC XT/AT compatible computer.

1.1 TIME CODE FORMATS

The widespread use of coded timing signals to assist in the correlation of intercept and test data began in the early 1950's. These signals can be decoded in real time to indicate the current time-of-day (TOD) or recorded along with intercept/test data on magnetic tape recorders for post processing and time correlation.

Hundreds of time code formats were developed, one for each agency involved. During the early 1960's the InterRange Instrumentation Group promoted a series of "standard" time code formats now loosely referred to as "IRIG Time Codes." The PC03XT decodes three of these formats: IRIG A, IRIG B, and IRIG G.

Several other formats still enjoy relatively widespread use within their originating agencies: NASA 36, XR3, and 2137. These codes are also processed by the PC03XT.

More complete details on these and other time code formats is available free of charge, on request from either Bancomm-Timing Division or Datum Inc in the form of the Datum Inc, Handbook of Time Code Formats.

1.2 RESOLUTION

Time of day is transmitted once per frame in an amplitude modulated coded signal. The PC03XT Time Code Reader Module decodes the TOD data, once per frame, and counts the number of carrier cycles from the start of the frame (the on time mark). PC03XT time resolution is therefore the period of the time code carrier. Table 1-1 details the frame period, carrier frequency and time resolution for each time code type.

Table 1-1
Time Code Resolution

Time Code Type	Frame Period	Carrier Frequency	Time Resolution
IRIG B	1 Second	1 kHz	1 millisecond
IRIG A	0.1 Second	10 kHz	100 microseconds
IRIG G	0.01 Second	100 kHz	10 microseconds
2137	1 Second	1 kHz	1 millisecond
XR3	1 Second	250 Hz	4 milliseconds
NASA 36	1 Second	1 kHz	1 millisecond

1.3 30 CHARACTER MESSAGE

In addition to time, IRIG A and IRIG B time code formats include three "control characters" per frame. Datum time code generators include a capability of encoding a 30 character alphanumeric message in these three control characters (a 30 character message is assembled in 10 frames). The PC03XT includes the capability of decoding this message if it is present in the IRIG A or IRIG B signals.

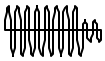
1.4 XT/AT COMPATIBILITY

AT type computers have an extended memory addressing capability over XT type computers. The PC03XT Time Code Reader Module is a port mapped device and therefore is not affected by this extended AT capability.

Physically, the PC03XT mounts in either an XT or AT type computer. In the case of the AT, the AT's second connector is not accessed or required by the PC03XT.

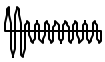
IRIG B Time Code Frame

Symbols:



Reference Mark: 8 HC, 2 LC

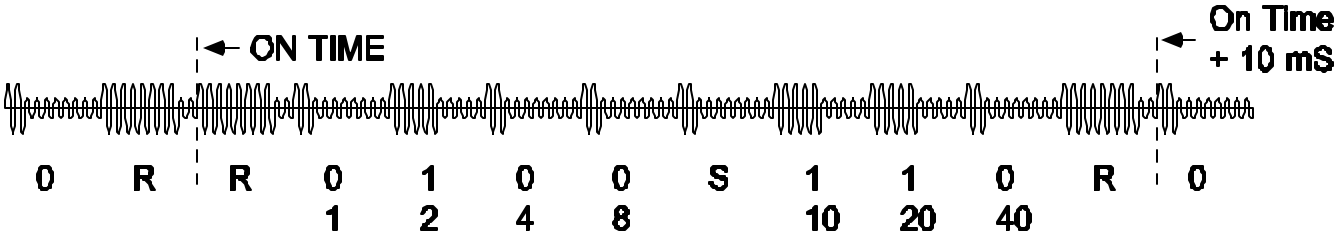
Logical '1': 5 HC, 2 LC



Logical '0' or Space: 2 HC, 8 LC

10 Cycles or 10 milliseconds for IRIG B or IEEE1344

On Time and First Sub Frame:



A double reference mark denotes the start of the frame, 'On Time'. Encoded BCD data is the time at On Time. The encoded data is this first subframe is 32 Seconds.

Frame:

IRIG B:

OT

R R SS R MM R HH R DD R D _ R C C R C C R C C R B B R B B R

Seconds
Minutes
Hours
Days
Control ***C***haracters
Control ***C***haracters
Control ***C***haracters
17 ***B***IT ***B***INARY TOD

CHAPTER TWO
SOFTWARE INTERFACE

2.0 GENERAL

The PC03XT Time Code Reader Module occupies a block of 32 bytes of PC I/O port address space. These port locations are used for setup information (time code type, forward/reverse, etc), requesting time capture, and the transfer of time code data. The block of addresses can be located on any one of the 16 32-byte blocks of I/O address space available in the XT/AT environment.

2.1 PC XT/AT BUS INTERFACE

The PC Bus allocates 512 bytes of I/O port addresses for plug-in boards located at address 200H - 3FFH. The PC03XT Reader Module uses a block of 32 I/O ports. Four position dip switch U35 is used to select the base address of the 32 byte block used by the reader. To select a base address, set each of the four dip switches to the ON or OFF position as shown in Table 2-1. Setting a dip switch to the ON position selects a logical zero for that address bit, and the OFF position selects a logical one (1).

Table 2-1
PC Bus Base Address Selection (U35)

		U35 DIP Switch								
		S1	S2	S3	S4					
Base Add	**A9**	**A8**	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
200H	1	ON	ON	ON	ON	0	0	0	0	0
220H	1	ON	ON	ON	OFF	0	0	0	0	0
240H	1	ON	ON	OFF	ON	0	0	0	0	0
260H	1	ON	ON	OFF	OFF	0	0	0	0	0
280H	1	ON	OFF	ON	ON	0	0	0	0	0
2A0H	1	ON	OFF	ON	OFF	0	0	0	0	0
2C0H	1	ON	OFF	OFF	ON	0	0	0	0	0
2E0H	1	ON	OFF	OFF	OFF	0	0	0	0	0
300H	1	OFF	ON	ON	ON	0	0	0	0	0
320H	1	OFF	ON	ON	OFF	0	0	0	0	0
340H	1	OFF	ON	OFF	ON	0	0	0	0	0
360H	1	OFF	ON	OFF	OFF	0	0	0	0	0
380H	1	OFF	OFF	ON	ON	0	0	0	0	0
3A0H	1	OFF	OFF	ON	OFF	0	0	0	0	0
3C0H	1	OFF	OFF	OFF	ON	0	0	0	0	0
3E0H	1	OFF	OFF	OFF	OFF	0	0	0	0	0

The I/O port function and location (relative to the base address) are shown in Table 2-2.

Table 2-2
PC Bus I/O Port Function and Location

Port Function	R/W	Port Location
Program Reader (0)	W	BASE + 00H
Program Reader (1)	W	BASE + 01H
Program Reader (2)	W	BASE + 02H
Program Reader (3)	W	BASE + 03H
Time/Msg. FIFO Data	R	BASE + 04H
Reset Time FIFO	R/W	BASE + 08H
FIFO Empty Flag (D0)	R	BASE + 0CH
Clear Interrupt	R/W	BASE + 10H
Time/Msg. Request	R/W	BASE + 14H
Reset Reader	R/W	BASE + 18H
Not Used	-	BASE + 1CH

Each port function is described in the following sections.

2.1.1 PROGRAM READER (0-3)

The first four port locations are used to select the various setup options. The setup information is written to a 4 X 4 register and therefore only data bits D0 - D3 are used. Table 2 - 3 shows the contents of these registers.

All bits that are not used should be set to zero for future software compatibility.

2.1.2 TIME/MSG FIFO DATA

The decoded time code or message data is transferred to the PC bus through an eight bit wide FIFO memory. Time data is sent if bit zero of PROGRAM READER (3) is set to zero and message data is sent if bit zero is set to one. The FIFO port is read only.

Each digit of time code is represented by one byte of data read from the FIFO. The format of the time code data is shown in Table 2 - 4. The upper four bits are used to determine which time code digit (days - hundreds, seconds - units, etc) is contained in the lower four bits (BCD encoded).

When reading time code data from the FIFO, the most significant time code digit (i.e., days - hundreds) is read out first and the least significant digit (i.e. 0.00001 sec) is read out last. When the time code error code (F1H) is read out, no time code data will be sent.

When reading message data from the FIFO, the message header byte (F2H) is read out first followed by the 30 message bytes in ASCII format. When the message error code (F3H) is read out, no message data will be sent.

Table 2-3
Program Reader (0)

D3	D2	D1	D0	Time Code Type
0	0	0	0	IRIG B
0	0	0	1	IRIG A
0	0	1	0	IRIG G
0	0	1	1	2137
0	1	0	0	XR3
0	1	0	1	NASA 36
0	1	1	0	Default to IRIG B (reserved for future code type implementation).
1	1	1	1	

Table 2-4
PROGRAM READER (1)

Bit	Function
1, 0	Select one of four input channels: 00 = Channel One 01 = Channel Two 10 = Channel Three 11 = Channel Four
2	Select Forward Or Reverse Operation 0 = Forward (Time Increasing) 1 = Reverse (Time Decreasing)
3	Not Used

Table 2-5
Program Reader (2):

Bit	Function
0	Hardware Triggered Time Request Sense 0 = Low To High Trigger 1 = High To Low Trigger
1	Hardware Triggered Time Request Enable 0 = Disable 1 = Enable
2	Not Used
3	Not Used

Table 2-6
Program Reader (3)

Bit	Function
0	Time/Message Request 0 = Request Time 1 = Request Message (IRIG A,B Only)
1-3	Not Used

Table 2-4
PDC & FIFO Data Format

D7	D6	D5	D4	D3	D2	D1	D0	Digit	Code
0	0	0	0	DH3	DH2	DH1	DH0	Days Hundreds	All
0	0	0	1	DT3	DT2	DT1	DT0	Days Tens	All
0	0	1	0	DU3	DU2	DU1	DU0	Days Units	All
0	0	1	1	0	0	HT1	HT0	Hours Tens	All
0	1	0	0	HU3	HU2	HU1	HU0	Hours Units	All
0	1	0	1	0	MT2	MT1	MT0	Minutes Tens	All
0	1	1	0	MU3	MU2	MU1	MU0	Minutes Units	All
0	1	1	1	0	ST2	ST1	ST0	Seconds Tens	All
1	0	0	0	SU3	SU2	SU1	SU0	Seconds Units	All
1	0	0	1	MSH3	MSH2	MSH1	MSH0	0.1 Seconds	All
1	0	1	0	MST3	MST2	MST1	MST0	0.01 Seconds	All
1	0	1	1	MSU3	MSU2	MSU1	MSU0	0.001 Seconds	All
1	1	0	0	USH3	USH2	USH1	USH0	0.0001 Seconds	IRIG A,G
1	1	0	1	UST3	UST2	UST1	UST0	0.00001 Seconds	IRIG G
1	1	1	0	-	-	-	-	Not Used	
1	1	1	1	*	*	*	*	See Below	All

* Error/Message Code

Table 2-8
Error/Message Codes

D3	D2	D1	D0	Code
0	0	0	1	Time Code Error
0	0	1	0	30 Byte Message Follows
0	0	1	1	Message Error

2.1.3 FIFO EMPTY FLAG (D0)

The FIFO empty flag can be read to determine when the FIFO contains time code data that can be read. When this port is read, data bit zero contains the empty flag status and data bits 1 - 7 are undefined. A logical zero indicates that the FIFO is empty, and a logical one indicates that the FIFO is not empty (i.e., contains one or more bytes of data). After a time request is issued (see TIME/MSG REQUEST) the FIFO empty flag must be read to determine when the time code data has been sent to the FIFO. This flag should be checked before each time code digit is read out of the FIFO. However, if interrupts are being used then the empty flag can be ignored because the interrupt is not generated until all the time data has been loaded into the FIFO.

2.1.4 RESET TIME FIFO

The time FIFO can be reset (emptied) at any time by accessing the RESET TIME FIFO port with a read or write. The FIFO should be reset following power-on or whenever the data in the FIFO is to be discarded.

2.1.5 TIME/MSG REQUEST

Time or the optional 30 character message can be requested by accessing the TIME/MSG REQUEST port with a read or write. The sense of bit zero in the PROGRAM READER (3) port determines whether time or message data will be sent (0 = Time, 1 =Message).

A read or write to the TIME/MSG REQUEST port freezes the time and begins the transfer of time to the FIFO. Approximately 300 microseconds later, the time or message data will become available when the FIFO empty flag goes false (logical one). See Section 2.13 for details on the empty flag.

2.1.6 CLEAR INTERRUPT

The interrupt line is cleared (i.e. reset to a logical zero) by accessing the CLEAR INTERRUPT port with a read or write.

2.1.7 RESET READER

The PC03XT Time Code Reader Module may be reset at any time by accessing the RESET READER port with a read or write. Resetting the reader does not change the contents of the PROGRAM READER (0-3) ports and does not affect the FIFO.

CHAPTER THREE
HARDWARE INTERFACE

3.0 GENERAL

The PC03XT Time Code Reader hardware interface consists of I/O connector(s) located on the card edge bracket, the Peripheral Data Connector (PDC), and the XT Bus edge connector.

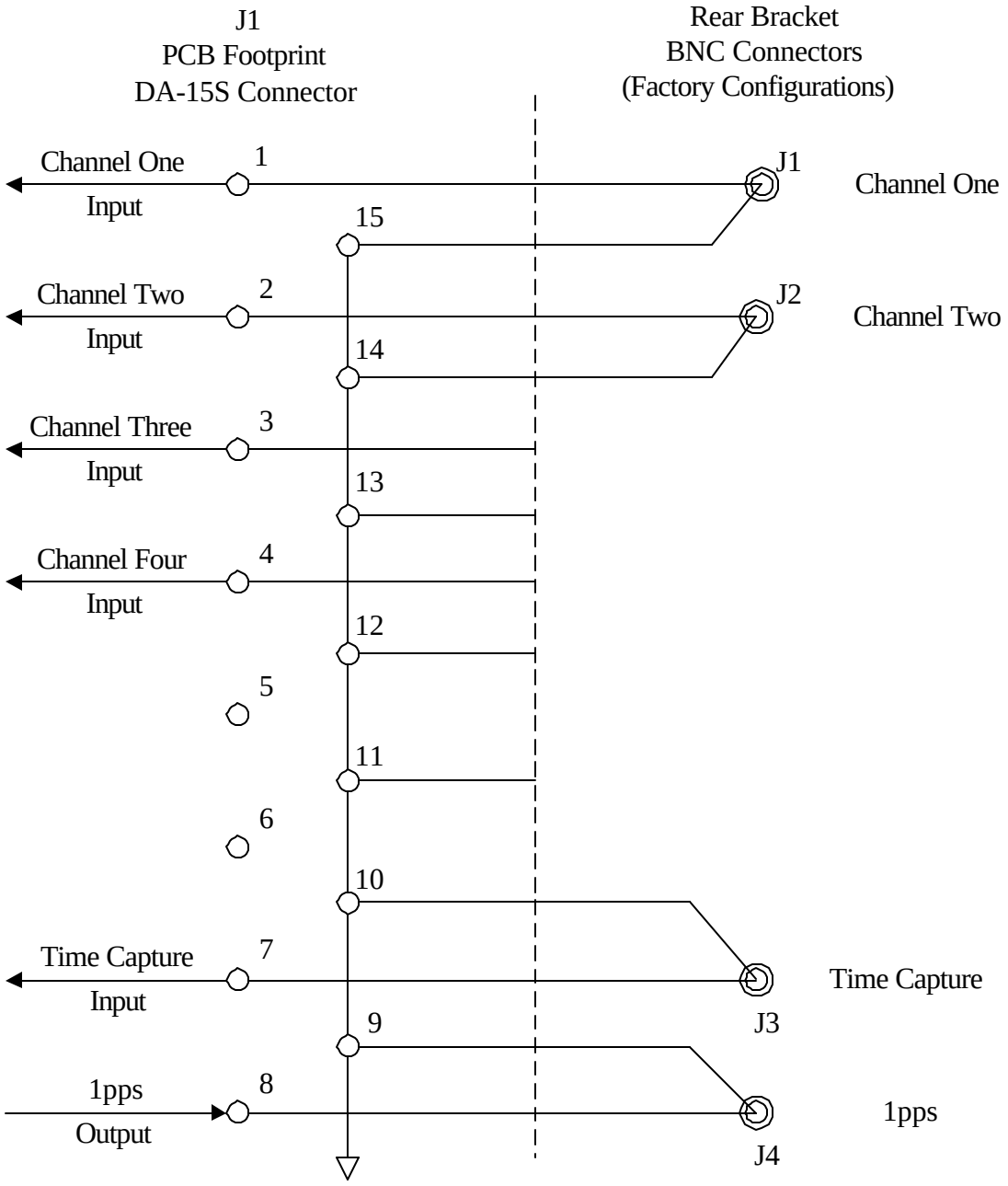
3.1 PC BUS EDGE CONNECTOR

The PC Bus edge connector is a 62 position connector that plugs into a PC XT/AT computer and contains the address, data, and control signals required to interface with the module.

3.2 REAR BRACKET CONNECTORS

The PC03XT Time Code Reader Module is designed to support either a 15 pin "D" type rear bracket connector (standard) or four rear bracket mounted BNC connectors (optional). Signals are available on the board at J1, a 15 pin "D" footprint, see Figure 3-1. If BNC connectors are used, the four desired signals are jumpered to the four rear bracket BNC's as shown in Figure 3 - 1. The user can alter this factory set configuration by unsoldering an undesired I/O line and re-soldering in the appropriate PCB J1 location.

Figure 3-1
PC03XT I/O Connections



3.2.1 TIME CODE INPUTS

The PC03XT is equipped with four software selectable time code input ports. Each input is terminated in 600 Ω.

3.2.2 TIME CAPTURE PULSE INPUT

In addition to requesting time by accessing the REQUEST TIME port, time can also be requested by applying a low to high (or high to low) TTL time capture pulse. The pulse must have a duration of at least 50 nanoseconds. Time will be frozen and sent to the FIF when the transition is detected. The Program Reader (2) port (see Section 2.11) controls the operation of the time capture pulse input.

3.2.3 1 PULSE PER SECOND (1pps) OUTPUT

A 1pps signal (TTL) is generated by the reader module for all time code types. This signal is a positive pulse whose duration is equal to one carrier cycle of the input code type (e.g. one millisecond for IRIG B, 100 microseconds for IRIG A, 10 microseconds for IRIG G). The low to high transition of this signal occurs within five microseconds of the time code "on time" mark. This signal can drive 75 Ω.

3.3 PERIPHERAL DATA CONNECTOR (PDC)

The Peripheral Data Connector is a 20 position rectangular connector located at the top of the Reader Module. This connector is used to transfer decoded time code data to other Datum Modules and to drive Datum display products. The pinout of this connector is shown in Table 3-1.

Table 3-1
PDC Pinout

Pin	Signal	Pin	Signal
1	GROUND	2	ENABLE*
3	D0	4	D1
5	D2	6	D3
7	D4	8	D5
9	D6	10	D6
11	Each Cycle	12	High Cycle
13	1 pps	14	Not Used
15	Not Used	16	Not Used
17	Frame Strobe	18	Ground
19	Not Used	20	+5 VDC

Decoded time code is transmitted once per frame using the ENABLE* and D0 - D7. D0 - D7 encoding is as per Table 2-4. Data should be latched into the peripheral device on the rising edge of ENABLE*.
EACH CYCLE is a TTL representation of the time code carrier (high during positive half cycles, low during negative half cycles). HIGH CYCLE is a TTL signal that is low during a portion of a positive high cycle.

Both 1pps and FRAME STROBE are TTL signals which are high during the first cycle of each 1pps interval and frame, respectively.

All PDC signals are capable of driving two TTL - LS loads.

3.4 INTERRUPT REQUEST JUMPER (JP1)

The PC Bus provides six active high interrupt lines for user interrupts (IRQ2 - IRQ7). Although some of these lines are generally dedicated to peripherals (disk drives, serial ports, etc.), access to any one of the six lines is provided.

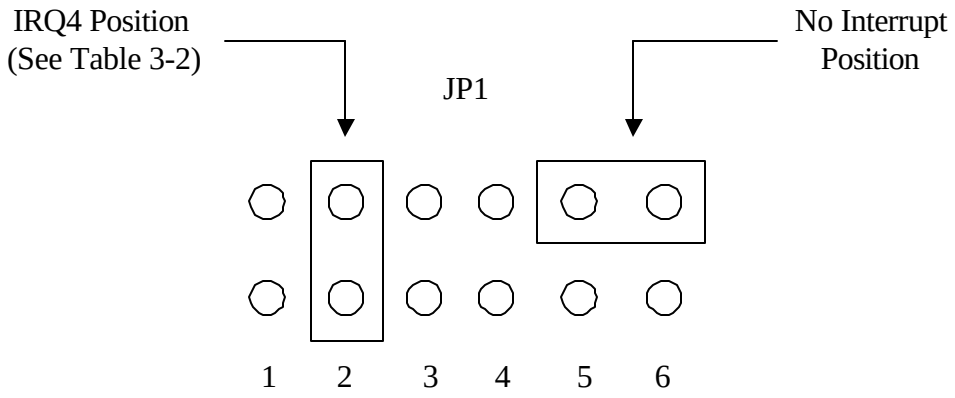
Jumper JP1 is used to select one of the six interrupt lines or to disconnect all interrupts for those applications that do not use interrupts. The jumper positions (1 - 6 with jumper mounted vertically) are shown in Table 3-2.

Table 3-2
JP1 Jumper Positions

JP1 Position	Interrupt Line
1	IRQ3
2	IRQ4
3	IRQ5
4	IRQ6
5	IRQ7
6	IRQ2

To disconnect the interrupts completely, place the jumper plug horizontally on the top row of JP1 or remove it from the board. Figure 3-2 shows the JP1 jumper.

Figure 3-2
JP1 Interrupt Line Jumper



CHAPTER FOUR
INSTALLATION

4.0 GENERAL

The PC03XT Time Code Reader Module is a full length XT size board designed to be installed in an IBM AT or XT computer or clone. A demonstration diskette is supplied with the module which is designed to run on MSDOS 3.2 or higher.

4.1 MECHANICAL INSTALLATION

- Remove the computer chassis cover.
- Select a vacant expansion slot and remove the blank rear panel bracket. Save the screw.
- Slide the PC03XT Time Code Reader Module straight down to engage the card edge guide at the front of the unit the card edge connector at the bottom.
- Fasten the top of the bracket to the chassis using the screw that was saved from the second step.
- Replace the chassis cover.

Note: If your PC03XT has BNC connectors the third step may not be possible without removing the top bracket screw on the PC03XT Time Code Reader and pushing the top of the bracket forward while installing the board. This is because the connector clearance on IBM machines and some clones is not sufficient to permit passage of the BNC connector which protrudes considerably further out than the "D" type or header normally mounted on expansion board brackets. After installation, the top bracket screw (which holds the top of the bracket to the PC03XT PCB) can be left off - the screw which holds the top of the bracket to the chassis is sufficient for most applications.

Because of the difficulty described above, Datum recommends the use of PC03XT's equipped with the 15 Pin "D" Connector Option.

4.2 DEMONSTRATION DISKETTE

This disk contains four executable programs that demonstrate the use of the PC03XT Reader Module.

IRIGA.COM	Reads IRIG A Time code
IRIGB.COM	Reads IRIG B Time code
IRIGG.COM	Reads IRIG G Time code
TCDEMO.EXE	General Purpose Demo Program for all time code types.

Instructions on the use of these programs is contained in the diskette file “README.DOC.” At the DOS prompt simply type “README.”

CHAPTER FIVE

SPECIFICATIONS

5.0 TIME CODE TYPES SUPPORTED

- IRIG A, B, G, 2137, XR3, and NASA 36.

5.1 CARRIER RANGE

- 125 Hz to 1 MHz.

5.2 DIRECTION

- Forward and Reverse.

5.3 MODULATION RATIO

- 2:1 to 6:1.

5.4 AMPLITUDE

- 400 mV to 10 Volts Peak-Peak.

5.5 TIME CODE INPUT IMPEDANCE

- 600 Ω.

5.6 TIME CAPTURE INPUT PULSE

- TTL, Rising Edge Active, 50 Ns minimum pulse width.

5.7 1 PPS STROBE ACCURACY

- Within five microseconds of "On Time."

5.8 TIME ACCESS LATENCY

- Time from "Request" to FIFO Data Valid - 300 microseconds.

5.9 SIZE

- Full Length PC-XT Compatible Plug-In.

CHAPTER SIX
DRAWING SET

6.0 DRAWINGS

Drawing Number	Pages	Title
11090	Four	Schematic Diagram CMOS Time Code Reader
11093	Two	Assembly, PC03XT CMOS Time Code Reader PCB

6.1 ANALOG PREPROCESSING

The analog preprocessing circuitry is shown on sheet one of schematic 11090.

One of four channels of time code is selected for decoding through an analog switch. The output of this switch is passed to an automatic gain control (AGC) circuit it equalize the level of the signal. The equalized signal drives two slices. One slicer generates a TTL level "each clock" cycle (high for the positive half of the cycle and low for the negative half of the cycle). The other slicer generates at TTL level "high cycle" signal which is low for a portion of the negative high amplitude cycle. These two signals drive the digital time code reader circuitry.

6.2 DIGITAL DECODER CIRCUITRY

The digital time code decoding circuitry is shown on sheet two of schematic 11090.

The "each cycle" and "high cycle" signals are the only signals needed to decode the time. First, a symbol clock is generated (U21) and used to clock the serial data into a shift register (U11, U20). The number of low cycles per symbol is counted (U40) and a 256 x 4RAM (U31) determines whether the symbol is a "one," a "zero," or a reference mark. Symbols are counted (U39, U42) and a 256 x 4RAM (U30) determines what to do with each symbol (i.e., shift it into the register, ignore it, etc.). When a complete digit is shifted into the shift register, it is latched into U23 and an interrupt is generated, telling the CPU that a digit is available. Consecutive reference marks are counted (U24) to determine the on time mark. An interrupt is generated when the on time mark is decoded.

6.3 CPU AND BUS INTERFACE

The CPU and PC Bus Interface circuitry is shown on sheet three of schematic 11090.

The Z80 CPU (U32) performs time validation (the time is considered valid when two consecutive frames have a one count difference) and formats the data into the PDC format. An 82C54 Counter-Timer-Chip (U33) counts the "each cycle" clock to obtain the frame sync signal. PDC data is buffered by U15 and PDC control signals are buffered by U16.

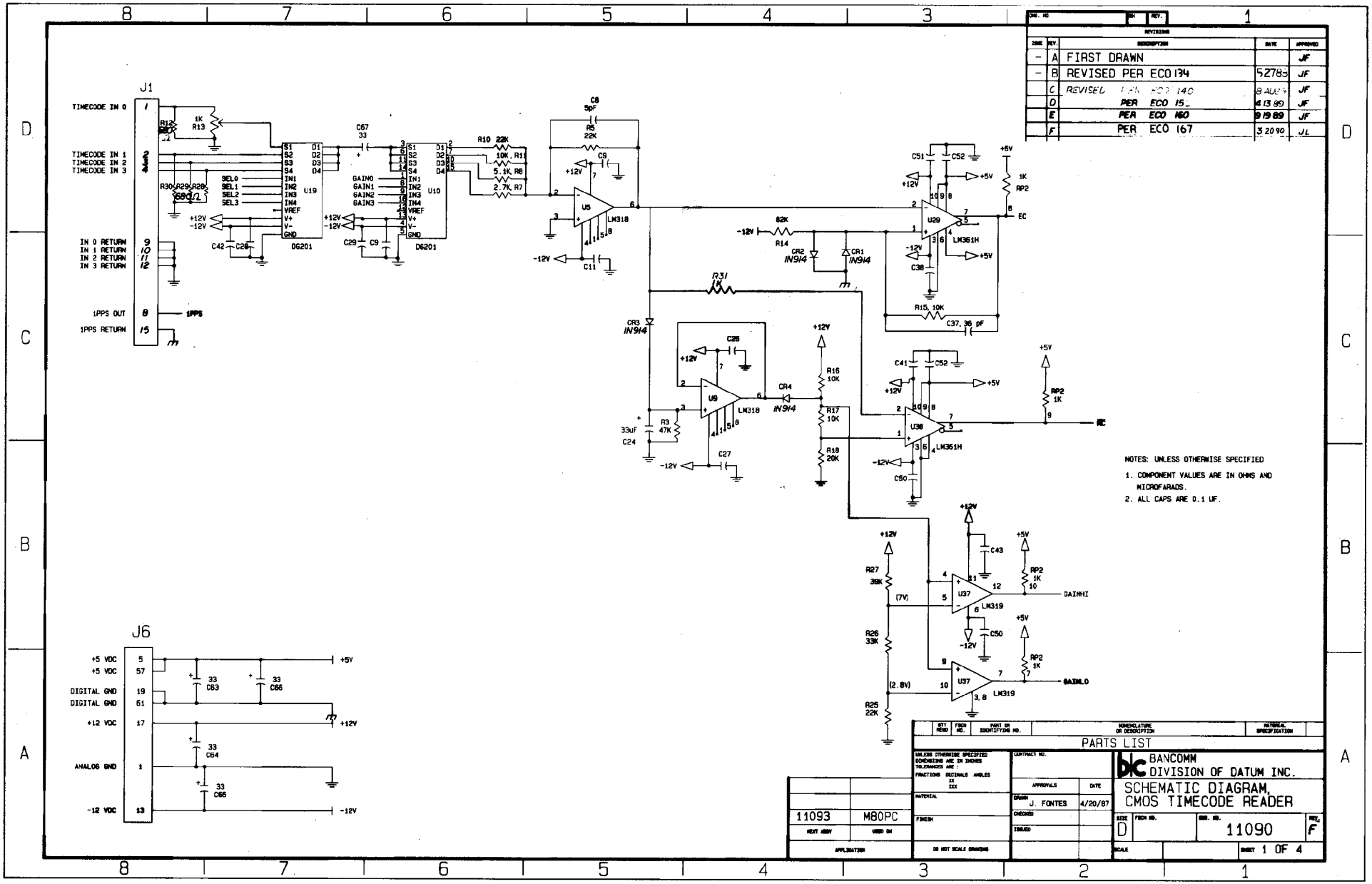
The PC bus interface consists of the address decoder section U36, U35, U2, U7, U28, the data FIFO (U47) and the reader control registers (U34). PC interrupts are generated by the U18 flip-flop.

6.4 EVENT TRIGGER CIRCUITRY

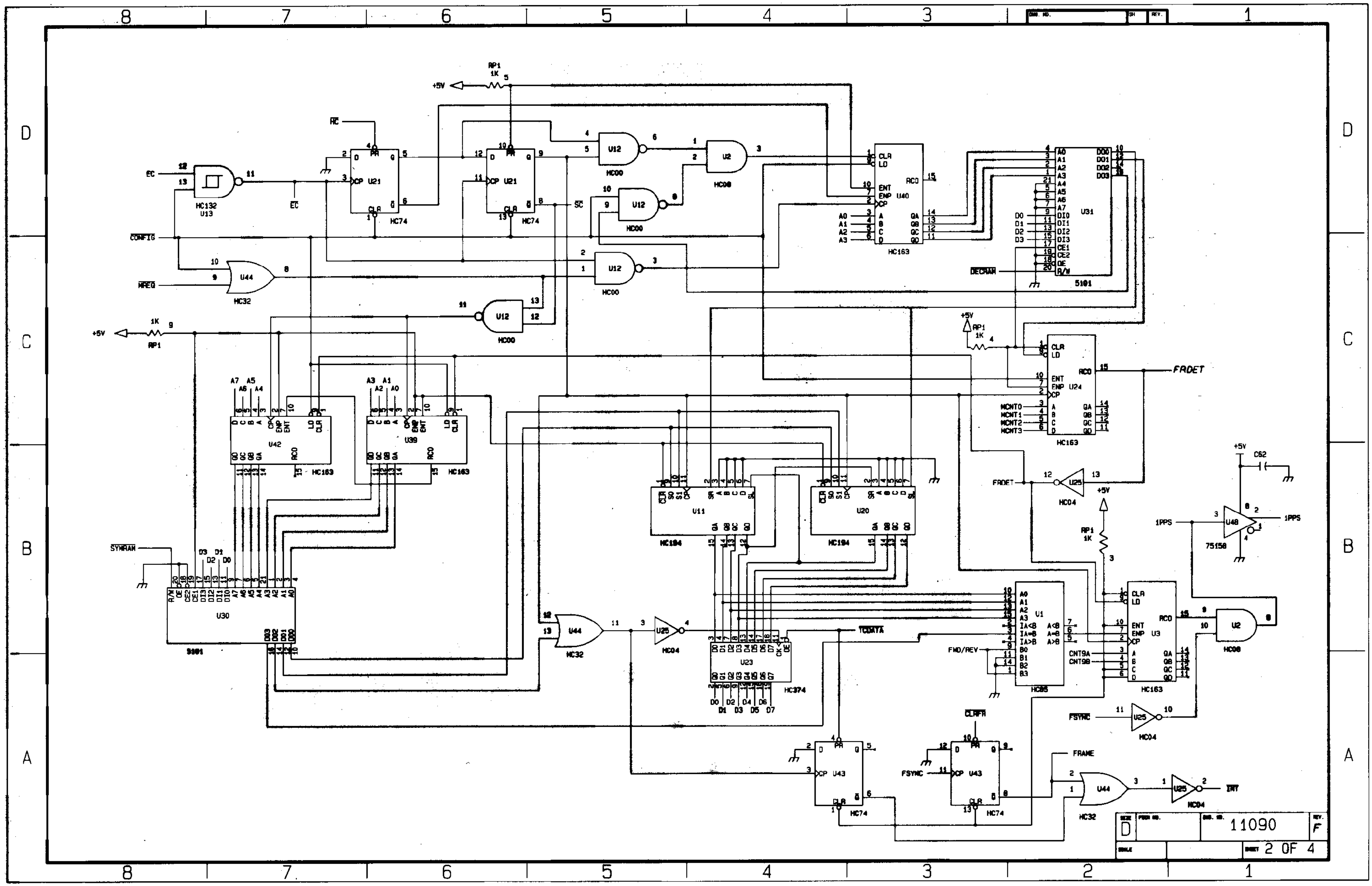
The event trigger circuitry is shown on sheet four of schematic 11090.

The external event is enabled by the U13 gate, inverted if necessary by U17 and converted to a pulse by U7, U6, R2, C10. The PC bus event trigger is OR'd with the external trigger pulse by U6. The event trigger is used to set the flip-flop U18 generating a non-maskable interrupt which tells the CPU to send the captured time to the PDC and time FIFO.

The U22 one-shot is used to reset the module from the PC bus. Counter U26 is used to count the "each cycle" clock for sub-second digits.



ZONE	REV.	DESCRIPTION	DATE	APPROVED
–	A	FIRST DRAWN		JF
–	B	REVISED PER ECO 134	52789	JF
	C	REVISED PER ECO 140	8 AUG 89	JF
	D	PER ECO 15_	4 13 89	JF
	E	PER ECO 160	9 19 89	JF
	F	PER ECO 167	3 20 90	JL



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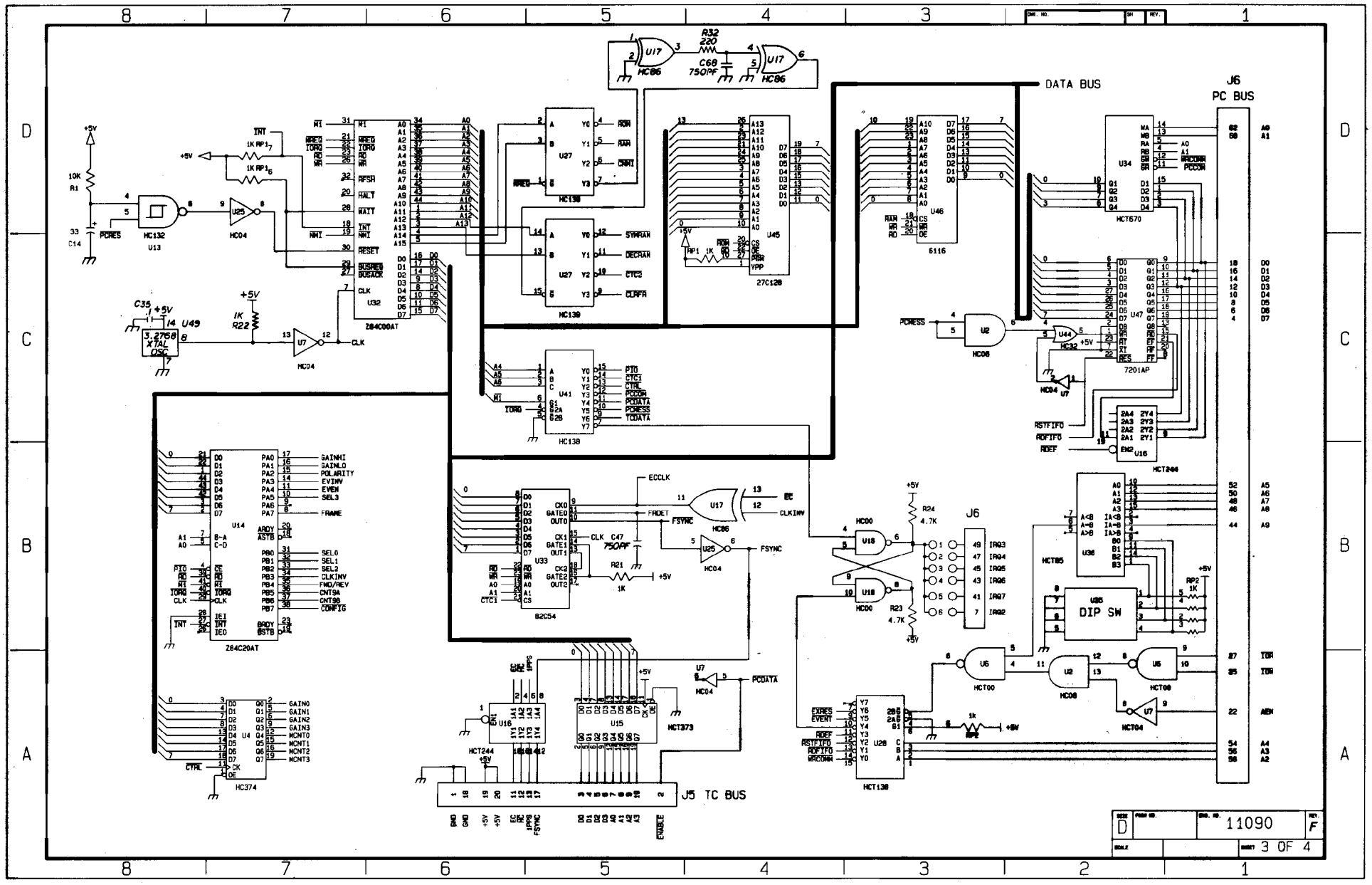
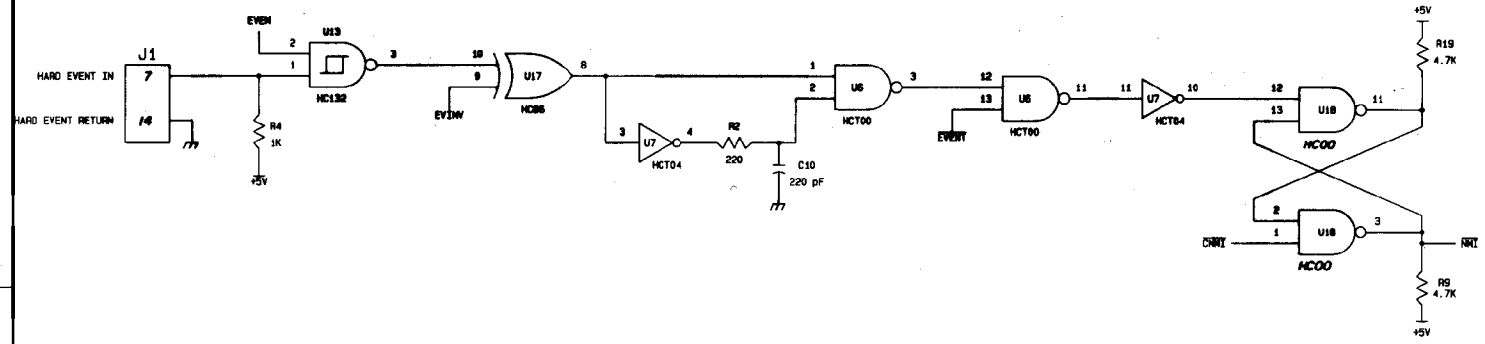
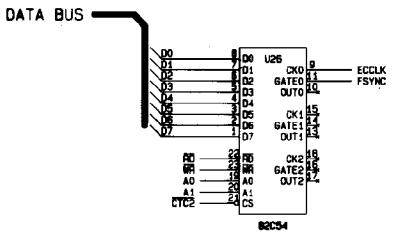
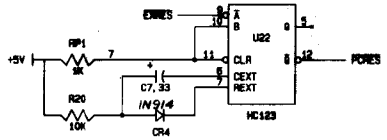
SCALE		SHEET 2 OF 4	


DATA BUS
J6
PC BUS
J5 TC BUS
DIP SW
11090
F
3 OF 4







SIZE D	FSCM NO.	DWG. NO. 11090	REV. F
SCALE		SHEET 4 OF 4	

REVISIONS				
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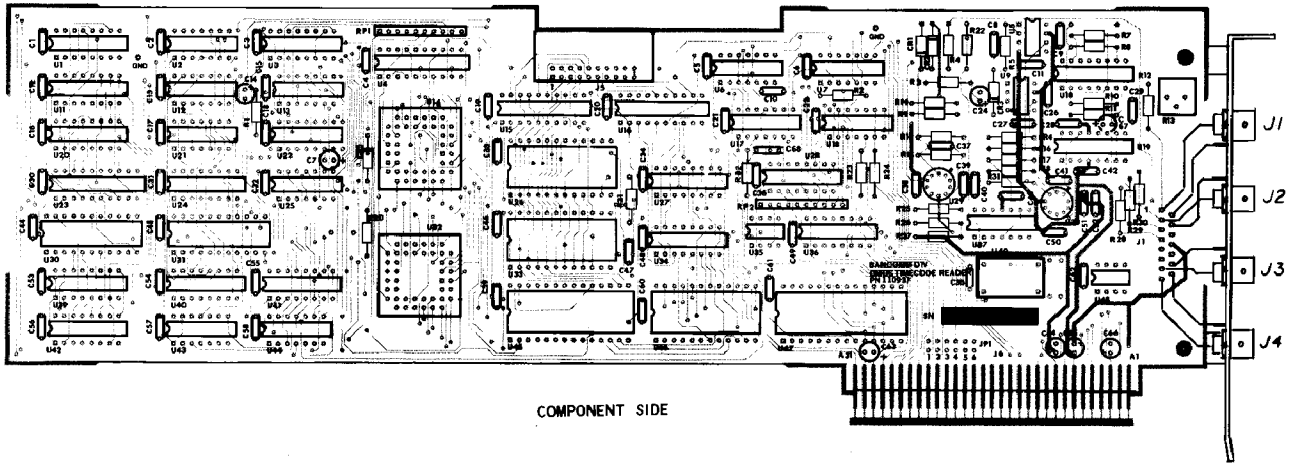
B		REV PER ECO No: 134	Mar 27,88	JF
C		REV PER ECO No: 140	Aug 8,88	JF
D		REV PER ECO No: 152	Apr 13,89	JF
E		REV PER ECO No: 160	Sep 19,89	JF
F		REV PER ECO No: 167	Mar 20,90	WW



COMPONENT SIDE

NOTE: OPTIONAL 15 PIN PCB CONNECTOR W/EXTERNAL CABLE, CAN BE INSTALLED IN J1, INSTEAD OF BNC's.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES XX — XXX — ANGLES —	CONTRACT NO.		BANCOMM DIV. of DATUM INC.
MATERIAL	PREPARED JL	DATE Mar 20,90	TITLE ASSEMBLY - PC03XT CMOS TIME CODE READER
	CHECKED WW	DATE Mar 21,90	
	APPROVED	DATE	
FINISH	APPROVED	DATE	SIZE C · CODE IDENT NO. UC-81 · 11093 · REV F
	APPROVED	DATE	SCALE NONE · SHEET 1 OF 2

PROJECT	NUMBER
NEXT ASSEMBLY	
APPLICATION	

Assembly, Parts Listing
PC03XT Time Code Reader

Ref: Drawing No: 11093 F

Ref: UC081

Mar 29, 1990

AS	OPT	BC P/N	MANF P/N	MANUFACTURE	VALUE	DESCRIPTION	QTY#	REF DESIG.
		1501050	CM05CD05D03	GI	5 PF, 500V	DIPPED MICA CAPACITOR	1.00	C8
		1501221	SCDM10FD221J	ARCO	220 PF, 500V	DIPPED MICA CAPACITOR	1.00	C10
		1501360	CM05ED360J03	ARCO	36 PF, 500V	DIPPED MICA CAPACITOR	1.00	C37
		1501751	CD15FC751J03	CDE	750 PF, 300V	DIPPED MICA CAPACITOR	2.00	C47,68
		1502104	SR265C104MAA	AVX	.1 MF, 50V	MONOLITHIC CERAMIC CAP.	24.00	C38-46,48-62
		1502104	SR265C104MAA	AVX	.1 MF, 50V	MONOLITHIC CERAMIC CAP.	29.00	C1-6,9,11-13,15-22,26-36
		1503336	336RMR025M	IC	33 MF, 35V	ALUMINUM ELECTROLYTIC CAP.	8.00	C7,14,24,63-67
		1701081	11092F	BANCOMM DIV, DAT	PC03XT Reader	PRINTED CIRCUIT BOARD	1.00	PCB-1
		2109020	3592-5002	3M	20 POS	RTANG HEADER	1.00	J5
		2117061	TSW-130-07-G-D	SAMTEC	2X30 POS	STRAIGHT TERMINAL STRIP	1.00	JP1 (CUT TO 2X6)
		2150028	10628-01-445	ANDON/SPECIRA	28 POS	DIP SOCKET	1.00	U45
		2152044	641747-2	AMP	44 POS	PLCC REC CHIP CARRIER	2.00	REF U14,32
		2155002	01-1021	E-MARK SYSTEMS		PCB TEST POINTS	2.00	GND
		2301003	C0-401A-0X	VECTRON	3.2768 MHZ	HYBRID DIP TTL OSCILLATOR	1.00	U49
		4701102	RC07GF102J	ALLEN BRADLEY	1 K OHM, 1/4W	FIXED RESISTOR	4.00	R4,21,22,31
		4701103	RC07GF103J	ALLEN BRADLEY	10 K OHM, 1/4W	FIXED RESISTOR	6.00	R1,11,15-17,20
		4701153	RC07GF153J	ALLEN BRADLEY	15 K OHM, 1/4W	FIXED RESISTOR	1.00	R3
		4701203	RC07GF203J	ALLEN BRADLEY	20 K OHM, 1/4W	FIXED RESISTOR	1.00	R18
		4701221	RC07GF221J	ALLEN BRADLEY	220 OHM, 1/4W	FIXED RESISTOR	2.00	R2,32
		4701223	RC07GF223J	ALLEN BRADLEY	22 K OHM, 1/4W	FIXED RESISTOR	3.00	R5,10,25
		4701272	RC07GF272J	ALLEN BRADLEY	2.7 K OHM, 1/4W	FIXED RESISTOR	1.00	R7
		4701333	RC07GF333J	ALLEN BRADLEY	33 K OHM, 1/4W	FIXED RESISTOR	1.00	R26
		4701393	RC07GF393J	ALLEN BRADLEY	39 K OHM, 1/4W	FIXED RESISTOR	1.00	R27
		4701472	RC07GF472J	ALLEN BRADLEY	4.7 K OHM, 1/4W	FIXED RESISTOR	4.00	R9,19,23,24
		4701512	RC07GF512J	ALLEN BRADLEY	5.1 K OHM, 1/4W	FIXED RESISTOR	1.00	R8
		4701823	RC07GF823J	ALLEN BRADLEY	82 K OHM, 1/4W	FIXED RESISTOR	1.00	R14
		4705102	710A102	ALLEN BRADLEY	1 K OHM, 1/8W	C-SIP RESISTORS, 10 PIN 'X'	2.00	RP1,2
		4803001	IN914			SILICON DIODE	5.00	CR1-5
		5108001	76SB04	GRAYHILL		4PST DIP SWITCH	1.00	U35
		9002602	74HC04	NATIONAL	14P DIP PKG	HEX INVERTER	1.00	U25
		9003642	74HC163	MOTOROLA	16P DIP PKG	SYNC 4 BIT BINARY COUNTER	5.00	U3,24,39,40,42
		9004632	74HC138	NATIONAL	16P DIP PKG	1 OF 8 DECODER/DEMUX	1.00	U41
		9004633	74HC139	NATIONAL	16P DIP PKG	DUAL 1 OF 4 DECODER/DEMUX	1.00	U27
		9004732	74HCT138	NATIONAL	16P DIP PKG	1 OF 8 DECODER/DEMUX	1.00	U28
		9006618	74HC74	NATIONAL	14P DIP PKG	DUAD D FLIP FLOP	2.00	U21,43
		9006658	74HC374	MOTOROLA	20P DIP PKG	OCTAL D FLIP FLOP	2.00	U4,23
		9007600	74HC00	NATIONAL	14P DIP PKG	QUAD 2-INPUT NAND GATE	2.00	U12,18
		9007606	74HC08	NATIONAL	14P DIP PKG	QUAD 2-INPUT AND GATE	1.00	U2
		9007615	74HC32	NATIONAL	14P DIP PKG	QUAD 2-INPUT OR GATE	1.00	U44
		9007623	74HC86	NATIONAL	14P DIP PKG	QUAD 2-INPUT EXOR GATE	1.00	U17
		9007630	74HC132	MOTOROLA	14P DIP PKG	QUAD 2-INPUT SCHMITT NAND GATE	1.00	U13
		9007700	74HCT00	MOTOROLA	14P DIP PKG	QUAD 2-INPUT NAND GATE	1.00	U6
		9007702	74HCT04	NATIONAL	14P DIP PKG	HEX INVERTER	1.00	U7
		9008757	74HCT373		20P DIP PKG	OCTAL D TRANSPARENT LATCH	1.00	U15
		9011627	74HC123	NATIONAL	16P DIP PKG	DUAL MULTIVIBRATOR	1.00	U22
		9013650	74HC194	NATIONAL	16P DIP PKG	4 BIT BIDIREC SHIFT REGISTER	2.00	U11,20
		9015622	74HC85	MOTOROLA	16P DIP PKG	4 BIT MAGNITUDE COMPARATOR	1.00	U1
		9015722	MC74HCT85N	MOTOROLA	16P DIP PKG	4 BIT MAGNITUDE COMPARATOR	1.00	U36
		9101010	TMPZ84C00AT	TOSHIBA	44P PLCC PKG	CMOS Z80 CPU	1.00	U32 (SKT)
		9103007	TMPZ84C20AT	TOSHIBA	44P PLCC PKG	CMOS Z80 PIO	1.00	U14 (SKT)
		9103008	82C54	AMD	24P DIP PKG .6	CMOS COUNTER TIMER	2.00	U26,33
		9201025	DG201BK	INTERSIL	16P DIP PKG	ANALOG SWITCH	2.00	U10,19
		9207070	SN75158P	TI	08P DIP PKG	DUAL 50 OHM TTL LINE DRIVER	1.00	U48
		9207715	74HCT244	NATIONAL	20P DIP PKG	OCTAL BUFFER/LINE DRIVER	1.00	U16
		9303015	LM319N	NATIONAL	14P DIP PKG	HIGH SPEED DUAL COMPARATOR	1.00	U37
		9303025	LM361H	NATIONAL	10P CAN PKG	COMPARATOR	2.00	U29,38
		9306025	LM318N	NATIONAL	08P DIP PKG	OP AMP, 8 PIN DIP	2.00	U5,9,
		9404015	7201SA120P	IDT	28P DIP PKG .6	FIFO 9X 512	1.00	U47
		9406308	27C128		28P DIP PKG .6	16 K BYTE EPROM	1.00	U45
		9407006	5101-30		22P DIP PKG	256 X 4 CMOS RAM	2.00	U30,31
		9407055	IDT6116SA150P	IDT	24P DIP PKG .6	8 X 2048 CMOS STATIC RAM	1.00	U46
		9407715	CD74HCT670E	RCA/HARRIS	16P DIP PKG	4 X 4 REGISTER	1.00	U34
	15D					ASSEMBLY OPTION		
	15D	1419004	10786A	BANCOMM DIV, DAT	PC03XT	IBM PC BRKT, 15 PIN CONNECTOR	1.00	BKT1
	15D	2123015	DAE15P	CANNON	15 POS	'D' PLUG	1.00	
	15D	2124015	747460-3	AMP	15 POS	'D' SOCKET, .59 RTANG PCB MNT	1.00	J1
	BNC					EXT. CABLE PARTS		
	BNC	2106001	31-317	AMPHENOL	50 OHM	BNC JACK, STRIGHT	4.00	CABLE PARTS
	BNC	2123015	DAE15P	CANNON	15 POS	'D' PLUG	1.00	CABLE PARTS
00						STANDARD ASSEMBLY 4BNC		
00		1419002	10784C	BANCOMM DIV, DAT	PC03XT	IBM PC BRKT, 4 BNC	1.00	BRKT1
00		2101003	31-221	AMPHENOL	50 OHM	FRONT MNT BNC BULKHEAD RECEP.	4.00	J1-4